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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/064,301  | 07/01/2002  | Jeffrey S. Brown     | BUR920010185        | 6395             |
| 24241   | 7590        | 04/02/2004           | EXAMINER            |                  |
| IBM MICROELECTRONICS<br>INTELLECTUAL PROPERTY LAW<br>1000 RIVER STREET<br>972 E<br>ESSEX JUNCTION, VT 05452 |             |                      | NGUYEN, THANH T     |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2813                |                  |
| DATE MAILED: 04/02/2004   |             |                      |                     |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**Application No. **10/064,301**Applicant(s) **BROWN ET AL.**Examiner **Thanh T. Nguyen**Art Unit **2813**

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 23 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 7 are stand rejected under 35 U.S.C. 102(b) as being anticipated by Cunningham (U.S. Patent No. 6,177,697) as previously applied.

Referring to figures 1-3B, Cunningham teaches a structure formed on a substrate comprising:

a plurality of isolation filled trenches (10) in a first region of the substrate (28/6, see figure 1 and col. 4, lines 39-61),

a plurality of holes (18, called “trench” in Cunningham) in the substrate (28/6), each having a plurality of sidewalls and a bottom wall (see figures 1, 2, and col. 4, lines 62-65), the holes adjacent to each other and located in a second region of a semiconductor substrate in which the plurality of isolation filled trenches (10) are absent, holes (18) having a depth proximate that of plurality of isolation filled trenches (10, see figure 1 and col. 6, lines 50-54),

insulating material (16, see col. 4, lines 40-41) present in each of the plurality of holes (18) on the plurality of sidewalls and bottom wall; and

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a conductor (22/23, see col. 6, lines 4-5) overfilling each of holes (18) and extending onto an adjacent upper surface of the substrate (28/6, see figure 1).

regarding to claim 2, a counter-doped region (6a, see figure 1 and col. 5, lines 58-63, and col. 6, lines 14-22, since region 6a having p-type dopant which is opposite to the n-type well region 28, hence region 6a is a counter-doped region) present in pillar regions of the semiconductor substrate (28/6) that surround the holes (18),

regarding to claim 3, a well region (28) located in semiconductor substrate (28/6),

regarding to claims 4 and 5, a transfer device (19, a field effect transistor, i.e. a gate electrode 19 formed on a gate oxide layer 16 having LDD source/drain regions p<sup>+</sup>, see col. 6, lines 3-13) located atop a surface of the semiconductor substrate (28/6) adjoining the plurality of holes (18),

regarding to claim 7, insulating material (16) is disposed on the upper surface of the substrate (28/6) beneath portions of conductor (22/23).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6 and 9 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (U.S. Patent No. 6,177,697) as applied to claims 1-5 and 7 above, further in view of Satoh (U.S. Patent No. 5,183,774) as previously applied.

Cunningham teaches an isolation trench (10) and holes (18) for capacitor in figure 1. However, Cunningham does not teach the insulating material is thicker on the bottom wall of the plurality of holes than on the plurality of sidewall of the plurality of holes, and an isolation dopant region is disposed below the bottom walls of the plurality of holes (as claimed in claims 6 and 9). Nevertheless, the insulating material is thicker on the bottom wall of the plurality of holes than on the plurality of sidewalls of the plurality of holes, and an isolation dopant region is disposed below the bottom walls of the plurality of holes is known in semiconductor art as evidenced by Satoh. Satoh teaches an insulating material (37, see figures 3D-3E and col. 5, lines 1-3) is thicker on the bottom wall of the plurality of holes (33, called "trench" for a capacitor in Satoh) than on the plurality of sidewalls (23) of the plurality of holes (33), and an isolation dopant region (36, called an "impurity layer" in Satoh) is disposed below the bottom walls of the plurality of holes (33, figures 3D-3E and col. 4, lines 65-68). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have an insulating material thicker on the bottom wall of the plurality of holes than on the plurality of sidewalls of the plurality of holes, and an isolation dopant region is disposed below the bottom walls of the plurality of holes in the device of Cunningham as taught by Satoh *because* a thicker insulating material formed on the bottom of capacitor holes (trenches) and an isolation dopant region formed below the bottom wall of capacitor holes (trenches) would provide an isolating region to prevent the charges which are stored in the capacitor from leaking into substrate.

Claims 8 and 10 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (U.S. Patent No. 6,177,697) as applied to claims 1-5 and 7 above, further in view of Tang (U.S. Patent No. 6,437,369) as previously applied.

Cunningham teaches an isolation trench (10) and holes (18) for capacitor in figure 1. However, Cunningham does not teach the holes have a depth greater than the plurality of isolation-filled trenches, the substrate has a buried insulation region and the plurality of holes extend into the buried insulation region (as claimed in claims 8 and 10). Nevertheless holes having a depth greater than the plurality of isolation-filled trenches, the substrate has a buried insulation region and the plurality of holes extend into the buried insulation region is known in semiconductor art as evidenced by Tang. Tang teaches holes (30, called "capacitor openings" in Tang, see figures 7-8 and col. 4, lines 5-23) have a depth greater than the plurality of isolation-filled trenches (24, see figures 2 and 7, and col. 3, lines 60-65, capacitor openings 30 are provided through SOI layer 16 into capacitor cell plate substrate 12 while isolation trench 24 is stop at insulating layer 14) and the substrate has a buried insulation region (14, beneath the semiconductive layer 16) and the plurality of holes (30) extend into the buried insulation region (14, see figure 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have capacitor holes having a depth greater than the plurality of isolation-filled trenches, and the substrate has a buried insulation region and the plurality of holes extend into the buried insulation region in the device of Cunningham as taught by Tang *because* a deeper capacitor hole would provide more capacitor area for storing charges, and buried insulating layer would provide more isolation for capacitor cell to prevent storage charges from leaking into substrate when capacitor hole extended into the buried insulating.

***Response to Arguments***

Applicant's arguments filed 1/8/04 have been fully considered but they are not persuasive.

Applicant contends that Cunningham does not teach or suggested isolation trenches are formed adjacent to each other and located in the second region. In response to applicant argument that Cunningham does teach the isolation trenches (10/42, see figures 1-2) are formed adjacent to each other and located the second region of the semiconductor substrate (44, see figure 2, col. 6, lines 37-43).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).



Thanh Nguyen  
Patent Examiner  
Patent Examining Group 2800